HIGH GAIN, HIGH EFFICIENCY, LOW VOLTAGE, MEDIUM POWER Si-BIPOLAR TRANSISTOR SUITABLE FOR INTEGRATION.

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Abstract—**Medium power transistors in a high performance double polysilicon bipolar process have been fabricated. On-wafer loadpull measurements show high gain (15 dB) and high maximum efficiency (60%) at 1.8 GHz with 27 dBm of output power. These results were obtained with a low supply voltage of 3.5 V. More importantly, these results were obtained with transistors with a buried layer having a collector contact at the top, which makes it possible to integrate power amplifiers on chip.**

INTRODUCTION

In the field of wireless communication, power amplifiers are an essential and critical building block of the system. Especially with the reduction in supply voltage (3.5 V) combined with higher frequencies (900MHz-1.8GHz) for communication standards like GSM, DECT, DCS-1800 it becomes more difficult to maintain the necessary high power gain and efficiency of power transistors.

For wireless applications very much attention in the literature has been paid to GaAs devices especially to the integration of PA's in RFIC's (see for example [1]). Also results were published for GaAs HBT's [2], HEMTs [3] or even SIC MESFETs [4] and SiGe HBT's. On the silicon front good results were obtained with lateral DMOS transistors [5]. However, not much has been published about silicon bipolar transistors as a power transistor for the 1.8 GHz area. This is surprising because a major performance improvement has occured in bipolar IC-processes in the last few years with the maturity of the double polysilicon bipolar process technology. Demonstrations of this process for front-end applications are presented numerously [6]. However, no results are known concerning power transistors in this kind of technology.

We already have shown [7,8] that high performance transistors can be fabricated in this technology. However, these were discrete types with a collector down configuration thus with a heavily doped substrate being the collector. In this paper we will demonstrate, for the first time, a high performance silicon bipolar transistor with an output power of 27 dBm at 1.8 GHz with a buried collector layer. This collector layer enables to contact the collector from above and isolates active area's. This has the advantage that more transistors can be integrated, an essential feature to make this a viable technology for future developments like RFIC's.

DEVICE FABRICATION

We have developed a high performance bipolar technology using a selfaligned double polysilicon transistor structure. The cross-section is shown in figure 1 and more details about the processing can be found in [7,8]. In this technology high cutoff frequencies of 25 GHz with a collector-emitter breakdown voltage of 5.0 V, can be readily achieved. With a small signal maximum available gain of 28 dB and a noise figure of 1.2 dB at 1.8 GHz, this is indeed a process highly suitable for front-end applications. To demonstrate the power capabilities of this process, we designed an output transistor for DECT-applications with an output power of 27 dBm. Figure 2 shows a photograph of the device

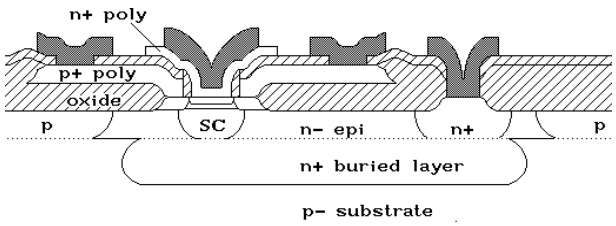

Figure 1: A schematic view of the cross-section of the double polysilicon bipolar technology in which the transistors were fabricated.

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with a total emitter length of 990 μm. The effective emitter width is about 0.4 μm accounting for a spacer width of 0.2 μm. Two Al metalization layers are used to contact the emitter, base and collector to the bondpads. In this configuration four emitter bonding wires can be used for die mounting.

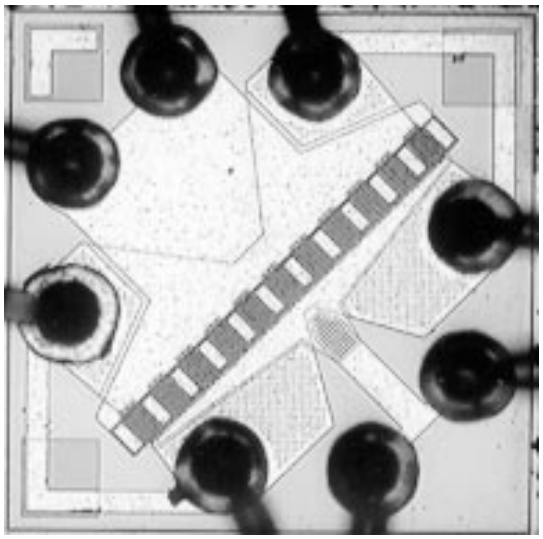

Figure 2: A layout of the 0.5 Watt bipolar transistor fabricated in the double polysilicon technology. Four bonding pads are used to contact the emitter.

MEASUREMENTS AND MODELING

Figure 3 shows the results obtained from on-wafer loadpull measurements at 1.8 GHz. The transducer gain and efficiency are shown for two tuning cases. The dashed lines are the results for a tuned output power of 27 dBm. High gain figures (15 dB at 1.8 GHz) and high efficiency (up to 60%) are obtained at a low supply voltage of 3.5 V. The solid lines in figure 3 are measured for a tuned output power of 28.5 dBm. The maximum efficiency remains the same and the power output capability increases significantly at the cost of lower peak gain.

These loadpull measurements are obtained with passive tuners from Maury and low-loss Cascade Microtech wafer probes are used to contact the transistor. The layout is a little different from figure 2 to facilitate GSG probe configuration. The transistor is biased class-AB with a base-emitter voltage of 0.7 V.

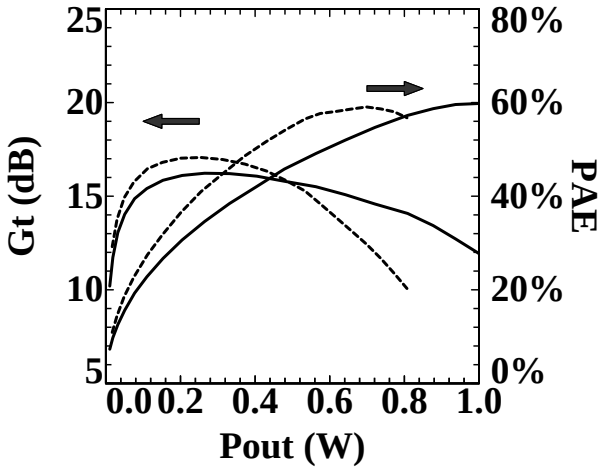

Figure 3: Measured large signal power gain and PAE for two tuning cases with a supply voltage of 3.5 V. Experimental results are obtained from on-wafer loadpull measurements.

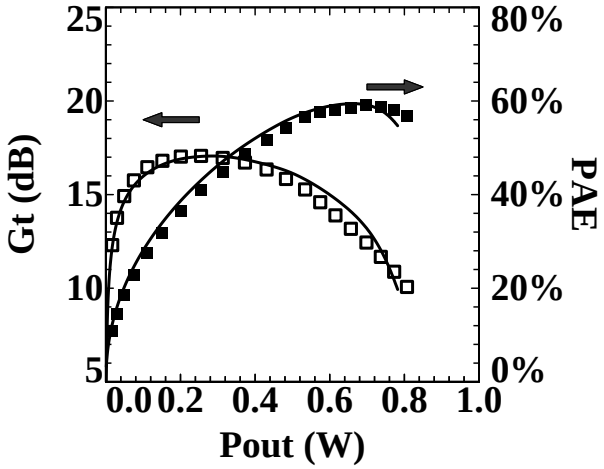

Figure 4: Comparison of measured large signal power gain and PAE (symbols) with simulations (lines) at 1.8 GHz as a function of output power with a supply voltage of 3.5 V. Experimental results are obtained from on-wafer loadpull measurements.

Figure 4 and 5 show the measured transducer gain and efficiency of the power transistor (symbols) for respectivelly 1.8 Ghz (tuned at 27 dBm) and 900 MHz. The drawn lines in figure 4 and 5 are the results of large signal harmonic balance simulations in MDS [9] using MEXTRAM [10,11] as a large signal bipolar compact model. The equivalent circuit of the MEXTRAM model is shown in

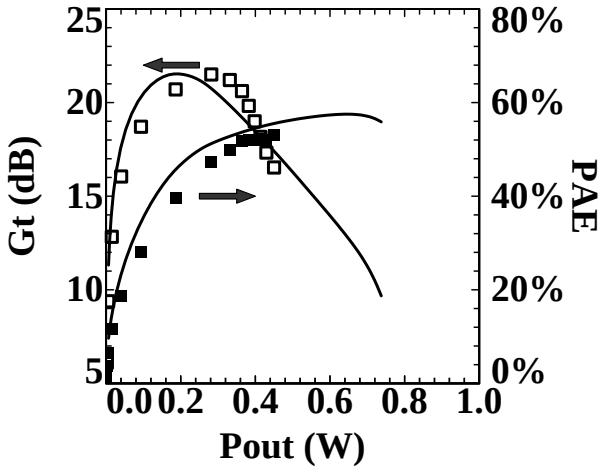

Figure 5: Comparison of measured large signal power gain and PAE (symbols) with simulations (lines) at 0.9 GHz as a function of output power.

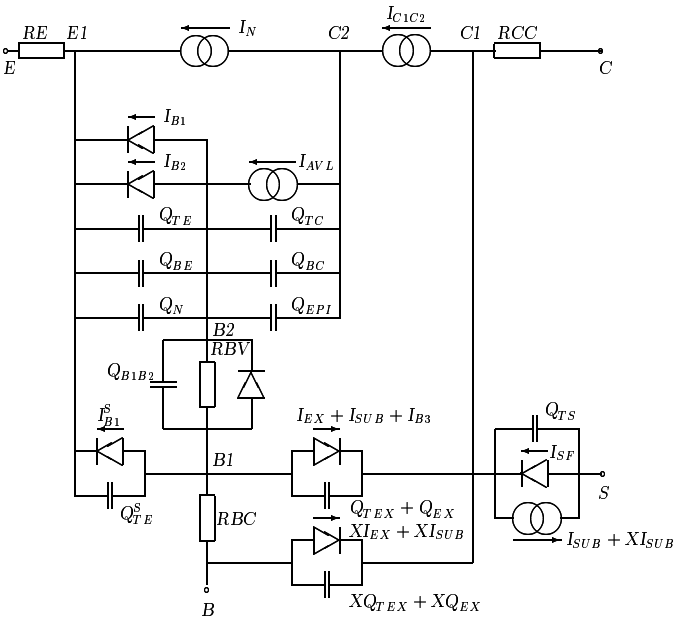

Figure 6: Compact bipolar model MEXTRAM used for large signal simulation of RF power transistors.

figure 6. This model is improved and implemented in MDS by [12]. Very good correspondence can be found between simulations and measurements. In the simulations the source and load impedances are taken from the measurement setup not only for the fundamental frequency but also for the second and third harmonic frequencies. This is essential for getting a good correspondence. Measurements and simulations also show that the use of a buried layer has no adverse effect on the RF-performance. This means that the collector resistance is kept sufficiently low by allowing 3 emitter fingers in one section. The influence of the buried layer is further investigated in figure 7. Here the RF performance of the transistor mounted in a SOT343R package is shown. The solid line is the result of a transistor with a buried layer and the dashed line is the result of a comparable transistor without a buried layer (collector down configuration). As can be seen, the

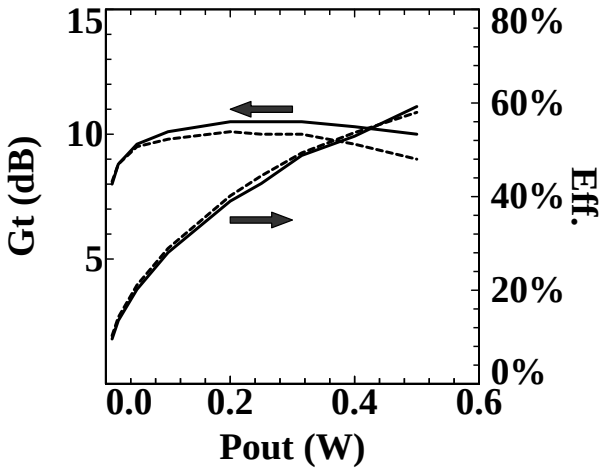

Figure 7: Measured large signal power gain and efficiency of transistor at 1.9 GHz mounted in the SOT343 package. Shown are the results for a buried layer type (solid lines) and without a buried layer (dashed lines).

efficiencies of both transistor almost coincide and no penalty in efficiency can be observed using the buried layer type. The gain of both transistors are reduced due to bonding parasitics, with the inductance of the emitter bonding wires being the most important one. An inductance of 0.2 nH is sufficient to explain the reduction in gain.

Finally, a two stage power amplifier for application as a predriver for GSM and DCS-1800 has been designed and processed. The amplifier, see figure 8 is fully integrated except for the output matching and can be used at 900 MHz and 1.8 GHz. At the same time, using these transistors in a package a gain of 30 dB has been realized in a two stage

power amplifier design on PCB.

CONCLUSIONS

As a conclusion, high performance bipolar transistors have been fabricated in a selfaligned double polysilicon process. The use of a buried collector layer has no adverse effects on gain and efficiency and shows that PA-RFIC's with bipolar technology are possible. The buried layer is also beneficial for discrete transistors.

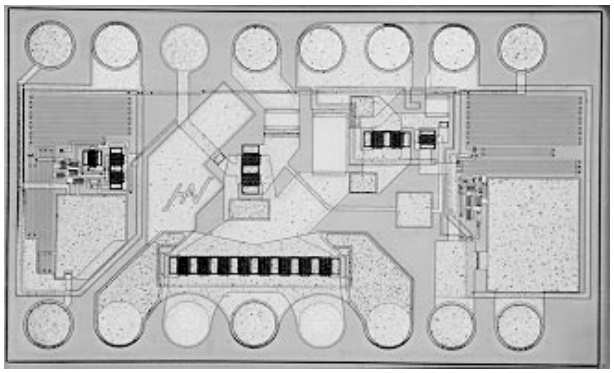

Figure 8: Photograph of a circuit of a fully integrated two stage power amplifier as a driver for GSM and DCS-1800 amplifiers.

ACKNOWLEDGEMENT

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[10] The MEXTRAM model, developed by Philips Electronics N.V. is public domain since 1994.
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